Low-Temperature Growth of Silicon Nanotubes and Nanowires on Amorphous Substrates

Beri N. Mbenkum,[†,‡] Andreas S. Schneider,[†] Gisela Schütz,[†] C. Xu,[§] Gunther Richter,[†] Peter A. van Aken,[†] Günter Majer,[†,‡] and Joachim P. Spatz[†,‡,*]

[†]Max Planck Institute for Metals Research, Heisenbergstr. 3, D-70569 Stuttgart, Germany, [‡]Department of Biophysical Chemistry, Im Neuenheimer Feld 253, University of Heidelberg, D-69120, Heidelberg, Germany, and [§]Oxford Instruments Plasma Technology, North End, Yatton, Bristol BS494AP, U.K.

ABSTRACT Silicon one-dimensional (Si 1D) materials are of particular relevance due to their prospect as versatile building materials for nanoelectronic devices. We report the growth of Si 1D structures from quasi-hexagonally ordered gold (Au) nanoparticle (NP) arrays on borosilicate glass (BSG) and SiO_x/Si substrates. Using hydrogen instead of oxygen plasma during NP preparation enhances the catalytic activity of AuNPs (diameters of 10−20 nm), enabling Si 1D growth at temperatures as low as 320 °C. On BSG, Si nanowires (SiNWs) are identified and reasonable vertical alignment is achieved at 420 °C. On SiO_x/Si, only Si nanotubes (SiNTs) are obtained right up to 420 °C. A mixture of SiNTs and SiNWs is observed at 450 °C and only SiNWs grow at 480 °C.

KEYWORDS: nanotubes · nanowires · nanoparticles · chemical vapor deposition

A fundamental goal of nanotechnology lies in the development of new materials with the aim of discovering novel properties to enable the creation of new technological systems and pitching the performance of contemporary ones. For commercial purposes, routes are sought which are straightforward and cheap. In this context, silicon one-dimensional (Si 1D) materials are a versatile choice[1] due to the eminence of Si-based devices in contemporary microelectronics. Furthermore, the noncytotoxic nature of Si makes it appealing for biotechnological applications.[2]

Si 1D materials such as nanowires (SiNWs) and nanotubes (SiNTs) have promising properties.[3−11] They are, for example, expected to serve as exciton splitting edges in future organic−inorganic photovoltaics.[12] Si 1D materials have a high surface-to-volume ratio, which is advantageous for the attachment of functional molecules.[13−15] The permeability of a SiNT may render it suitable for chemical sensors and molecule incorporation for controlled therapeutic agents. The potential of these materials can be exploited economically if the template structuring and Si 1D synthesis are achieved in a cost-effective manner on cheap and flexible substrates.

Si 1D growth processes typically require synthesis temperatures around 500 °C,[16−18] which are not conducive for growth on materials with low melting points. Low-temperature Si 1D growth is achievable *via* the use of small diameter nanoparticle (NP) seeds such as gold (Au) because they possess a large surface-to-volume ratio with unstable and lowly coordinated surface atoms.[19,20] This configuration helps to lower the melting point of NPs and enhance their catalytic activity, thus enabling growth at temperatures below 500 °C and even beneath the Au−Si eutectic temperature.[21,22] NPs also dictate the diameter and position of the Si 1D structures on substrates[23]—a crucial asset for pitching device performance. Several NP synthesis routes have previously been developed.[24−29] A critical factor in the synthesis of NPs is their defined placement on substrates. Micelle nanolithography[26,30,31] is an adequate tool for the preparation of monodisperse NPs in that it enables a fine control over their size and lateral spacing on substrates *via* a self-assembly route. The technique is applicable to large surface areas on nearly any wetable substrate, and NP feature sizes can be achieved well below 10 nm.

Substantial effort has been invested in achieving the growth of SiNWs from NPs at low temperatures.[22,32,33] Although SiNTs have been synthesized in the past,[34−41] a well-regulated, low-temperature NP-mediated SiNT route has not been accomplished so far, and this has strongly affected the selectivity of the growth process and the precise control over SiNT size. The challenge in the directed assembly of SiNTs lies in the sp^3 hybridization of Si, which favors a diamond-like structure, thereby leading to

*Address correspondence to spatz@mf.mpg.de.

Received for review August 9, 2009 and accepted February 24, 2010.

Published online March 10, 2010.
10.1021/nn900969y

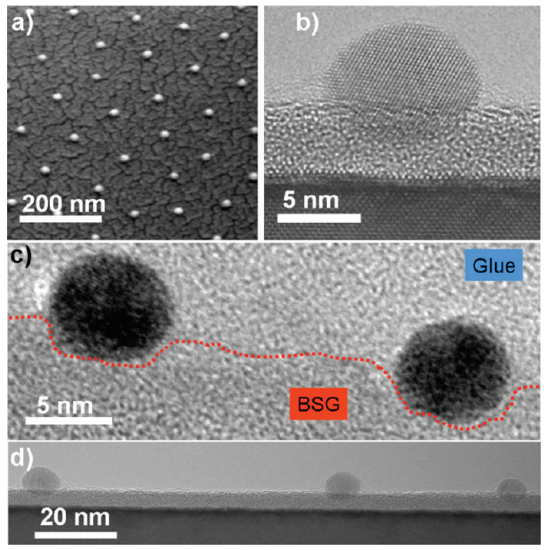

Figure 1. Electron micrographs of Au nanoparticles on BSG and SiO_x/Si substrates: (a) SEM images showing a tilted view (45°) of AuNPs arranged in a quasi-hexagonal order on a BSG substrate. The Au NPs are arranged in a quasi-hexagonal order with diameters of $D \sim 15$ nm and a lateral spacing of $L \sim 100 \pm 20$ nm. The rough textured surface between the AuNPs on the BSG substrate is due to the Au thin film layer sputtered in order to facilitate imaging on the nonconductive surface; HRTEM images of Au NPs on SiO_x/Si (b,d) and BSG (c) substrates after a H_2 plasma burning process. (b) Zoom-in image of a AuNP with a diameter of about 9 nm. The amorphous features on the NP surface are presumably remnants of glue from the sample preparation process. The particle is partly embedded in an amorphous SiO_x layer. (c) AuNPs partially embedded in a topographically rough BSG substrate as compared to the relatively flat SiO_xSi substrate shown in panel d.

the classical SiNW formation in a NP-mediated Si 1D growth process.

This paper concerns the growth of Si 1D structures on amorphous substrates *via* a NP-mediated route at temperatures ranging from 320 to 480 °C on BSG and SiO_x/Si substrates. We achieve growth *via* dissociative adsorption of monosilane (SiH_4) on gold (Au) NPs. The catalyst-mediated route, on the basis of micelle-prepared NPs, is chosen with the essential motive of lowering synthesis temperature and synthesizing Si 1D structures with well-defined size and spacing, with an eventual boost in Si 1D material yield. A model suggesting the origin of the experimental observations is discussed.

RESULTS AND DISCUSSION

A representative scanning electron microscopy (SEM) image of the typical AuNP pattern obtained from micelle nanolithography[25,26] is depicted in Figure 1a. The AuNPs, in this case on BSG, have diameters of $D \sim 15$ nm and are arranged in a quasi-hexagonal order and a mean lateral spacing of $L \sim 100 \pm 20$ nm. A zoom-in on the AuNPs reveals their crystalline nature, as shown in the HRTEM image of Figure 1b. High-resolution transmission electron microscopy (HRTEM) images illustrating a cross-sectional view of the Au/BSG and Au/SiO_x/Si microstructures are depicted in Figure 1c,d, respectively. We observe AuNPs partially embedded in both BSG and SiO_x/Si substrates, with embedment depths of approximately 1/3 of the NP radius (Figure 1b). The SiO_x surface appears topologically flat as compared to the relatively rough BSG surface whereby, alongside partial embedment, the NPs are observed to lie in crevices of different altitude.

When using an O_2 plasma during NP preparation, temperatures above 480 °C (550 °C) were generally required to activate Si 1D growth from 6 nm (10 nm) AuNPs. In the case of a H_2 plasma treatment, we discovered appreciable Si 1D growth at temperatures as low as 320 °C from 10 nm AuNPs. The results presented here are based on experiments performed with NPs prepared in H_2 plasma. Within the frame of our experiments, Si 1D growth was not readily achieved at temperatures below 400 °C from larger AuNPs ($D > 15$ nm). For NPs with $D \leq 15$ nm, the specific size had negligible impact on the low-temperature Si 1D growth process. Figure 2 shows the Si 1D structures grown on BSG (top row, Figure 2a−c) and SiO_x/Si (bottom row, Figure 2d−f) substrates at 320 °C (Figure 2a,d), 350 °C (Figure 2b,e), and 420 °C (Figure 2c,f). The growth time was 5 min, and the growth rate was found to increase with ascending synthesis temperatures as observed in previous studies.[22,42] Several Si 1D structure morphologies are observed at the different growth temperatures. We identify worm-like features, which grow parallel to the substrate surface, kinked structures which grow out of plane, and straight ones. At a growth temperature of 320 °C, Si 1D structures are worm-like on both BSG (>99%) and SiO_x/Si (>95%) substrates (Figure 2a,d) with projected lengths, l, on the order of 100 nm. The Si 1D diameter, $d \sim 10$ nm, is dictated by the small size of the NPs ($D \sim 10$ nm), which were chosen to enable Si 1D growth at these low temperatures. Figure 2b,e shows Si 1D structures grown at 350 °C from slightly larger AuNPs with diameters of approximately 12 nm. On both BSG and SiO_x/Si substrates, Si 1D structures of similar size and length ($d \sim 14$ nm; $l \sim 120$ nm) are obtained. Some of the Si 1D structures are kinked (<10% on BSG and >80% on SiO_x/Si), while others adopt the same growth pattern and morphology (>90% on BSG and <10% on SiO_x/Si) as those acquired at 320 °C. Alongside these structures, a few straight and vertically aligned ones are observed on both BSG and SiO_x/Si substrates. Figure 2c,f shows the corresponding Si 1D structures grown at 420 °C. Approximately 90% of the Si 1D structures ($d \sim 14$ nm; $l \sim 2$ μm) on BSG are straight and grow at a maximum inclination angle of 40° to the substrate normal. The structures bend, most likely under the interactions implemented by the electron beam, but are mainly vertically aligned, as shown in the cross-sectional view in the lower inset of Figure 2c. The strong oscillation of the Si 1D structures in the electron beam is most likely due to their small diameter

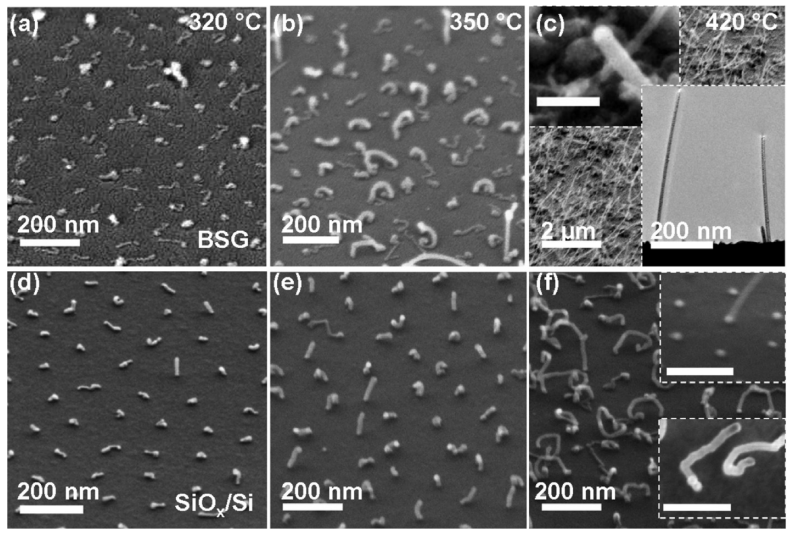

Figure 2. SEM images of Si 1D structures on BSG (top row) and SiO_x/Si (bottom row) substrates grown for 5 min at 320 °C (a,d), 350 °C (b,e), and 420 °C (c,f). At 320 °C, Si 1D structures ($d \sim 10$ nm; $l \sim 100$ nm) are worm-like and grow parallel to the surface of both BSG (>99%) and SiO_x/Si (>95%) substrates. At 350 °C, the Si 1D structures ($d \sim 14$ nm; $l \sim 120$ nm) are kinked (<10% on BSG and >80% on SiO_x/Si) and grow out of plane. Some Si 1D structures adopt the same growth pattern and morphology (>90% on BSG and <10% on SiO_x/Si) as those acquired at 320 °C. A few straight and vertically aligned ones are observed on both BSG and SiO_x/Si substrates. On BSG (c) at 420 °C, ~90% of the Si 1D structures ($d \sim 14$ nm; $l \sim 2$ μm) are straight and grow at a maximum inclination angle of 40° to the substrate normal. The lower right inset in panel c shows vertically aligned Si 1D structures on BSG. The top left inset shows a NP at the tip of a Si 1D structure, indicating tip-growth mode. At 420 °C on SiO_x/Si (f), the Si 1D structures grow shorter ($d \sim 12$ nm; $l \sim 200$ nm) than those on BSG and are mainly kinked (~90%) in nature. A few worm-like Si 1D structures (~10%) are also observed. The top inset in panel f shows a root-growth mode, and the bottom inset indicates the rounded nature of the Si 1D structure. The unlabeled scale bars in the insets of panels c and f all correspond to 100 nm.

as larger Si 1D structures ($d > 20$ nm - not shown) do not oscillate in the same manner when exposed to the same imaging conditions. Kikkawa *et al.* observed a similar temperature-dependent morphological evolution for SiNWs grown on Si,[42] as illustrated in our work for structures grown on BSG. A closer examination reveals that the AuNP which promoted growth is situated at the tip of the Si 1D structure (tip-growth mode), as exemplified in the top inset of Figure 2c (from a carbon-coated sample). Contrary to this situation, on the SiO_x/Si substrate, the Si 1D structures grow shorter ($d \sim 12$ nm; $l \sim 200$ nm) than those on BSG and are mainly kinked (~90%) in nature. A few worm-like Si 1D structures (~10%) are also observed to occur. The top inset of Figure 2f is a high-resolution SEM image which shows that the AuNP is located at the bottom of the Si 1D structure (root-growth mode). The bottom inset (Figure 2f) shows the top of a Si 1D structure without a NP at its tip, further confirming the root-growth mode. Compared to a global view, the yield obtained on BSG for Si 1D structures ($d \sim 14$ nm; $l \sim 2$ μm) grown in a tip mode is an order of magnitude higher than that acquired on SiO_x/Si ($d \sim 14$ nm; $l \sim 200$ nm) in a root mode. This observation is very interesting as the Si 1D structures on both BSG and SiO_x/Si samples were produced together at the same time under identical growth conditions within the same growth chamber.

To gain profound knowledge on the crystalline nature of the Si 1D structures synthesized on SiO_x/Si, we studied the growth process in more detail and extended the temperature range to 480 °C. The growth time was prolonged to 15 min to acquire more material for TEM analysis. The top row of Figure 3 shows SEM images of Si 1D structures grown at 350, 450, and 480 °C for 15 min. The structures have estimated lengths ranging up to 10 μm, hence demonstrating the high yield also achievable at temperatures as low as 350 °C. When the temperature is increased from 350 to 450 °C, only a slight enhancement of the yield is observed, but this significantly increases as the temperature is raised to 480 °C. The bottom row of Figure 3 shows corresponding TEM images of Si 1D structures grown at temperatures of 350, 450, and 480 °C. The Si 1D structures acquired at 350 °C (Figure 3d) show bright contrast in the interior of the crystals, which is indicative of hollow/tubular Si 1D structures. The structures look morphologically similar to SiNTs achieved *via* self-assembly[38] and laser ablation[41] techniques. Exclusively such structures occur in our system at temperatures below 450 °C. At 450 °C, we observe elongated Si 1D structures with rounded tips, dark side walls, and a bright contrast in the middle indicating a hollow structure. Although the structures shown in Figure 3e are hollow-like in nature, a mixture of hollow and filled (one of such is indicated in Figure 4f) Si 1D features were observed at 450 °C. At a growth temperature of 480 °C (Figure 3f), only filled structures are found.

HRTEM investigations revealed the structures grown on BSG to be SiNWs (not shown herein). To approve the aforementioned filled/hollow nature of the Si 1D

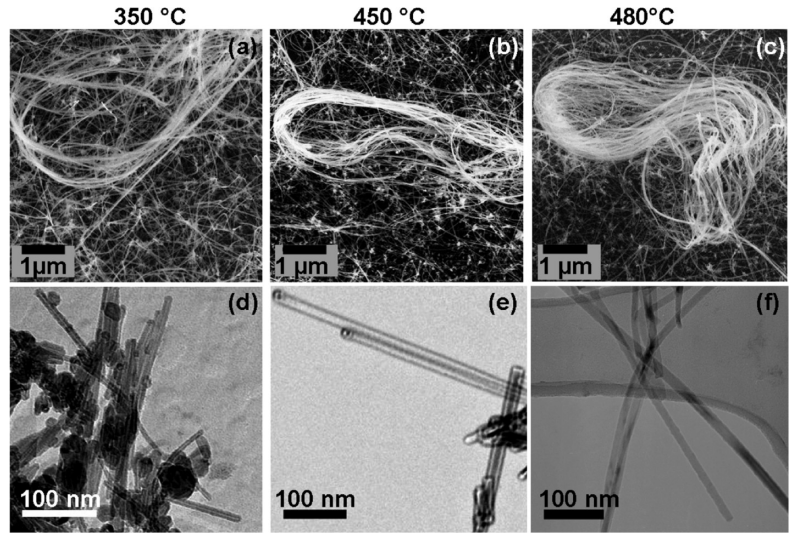

Figure 3. SEM (a−c) and TEM (d−f) images of Si 1D structures grown on SiO_x/Si at 350 °C (a,d), 450 °C (b,e), and 480 °C (c,f) for 15 min. The SEM images reveal the high yield of Si 1D material at 350 °C, which is comparable to that obtained at 450 °C. Si 1D yield is higher at 480 °C. The Si 1D structures attain lengths ranging up to approximately 10 μm. In the bottom row (d−f), Si 1D structures with dark side walls and a bright contrast in the middle appear to be hollow in nature at 350 °C. The nature of the Si 1D structure grown at 450 °C (e) with bright outer walls and a dark contrast in the middle is not very apparent. At 480 °C, only "filled" Si 1D structures are observed.

structures grown on SiO_x/Si substrates, HRTEM investigations were performed on several species grown at 350 °C (Figure 4a−c), 420 °C (Figure 4d−e), and 450 °C (Figure 5f−h). The structures indicated in Figure 4a−e are revealed to be SiNTs with diameters of 10, 12, 13, 14, and 18 nm grown from NPs of the same diameter. All of these SiNTs have a wall thickness of approximately 4−5 nm. The SiNTs are multiwalled with aligned and slightly distorted lattice fringes. Si 1D structures with diameters of 14, 18, and 22 nm, which were grown at 450 °C, are depicted in Figure 4f−h. Crystalline NWs are obtained from NPs with diameters of $D < 15$ nm, as

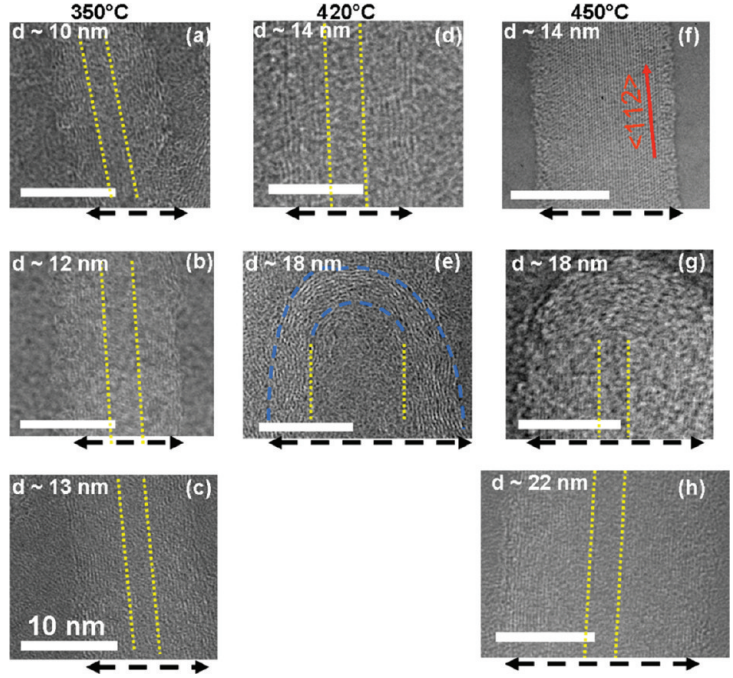

Figure 4. HRTEM images of Si 1D structures grown on SiO_x/Si substrates. (a−c) Multiwalled SiNTs acquired on SiO_x/Si at 350 °C with total diameters of 10, 12, and 13 nm and a wall thickness of approximately 4−5 nm; (d,e) 14 nm SiNT and the rounded tip of an 18 nm wide SiNT both grown at 420 °C (blue dashed lines highlight the rounded nature of the 18 nm SiNT tip); (f) 14 nm wide SiNW grown at 450 °C on a SiO_x/Si substrate with the wire axis along the ⟨112⟩ crystallographic direction. The lattice fringes in (f) of the SiNW are seen to occur throughout the complete diameter of the crystalline structure, thus confirming its "filled" nature. (g,h) SiNTs (18 and 22 nm wide) grown at 450 °C on SiO_x/Si. The inner wall diameter of the SiNTs is demarcated by the yellow dotted lines, while the black dashed lines indicate the total diameter of the Si 1D structures. SiNT growth on SiO_x/Si shows strong correlation with NP size and growth temperature. The scale bars all correspond to 10 nm.

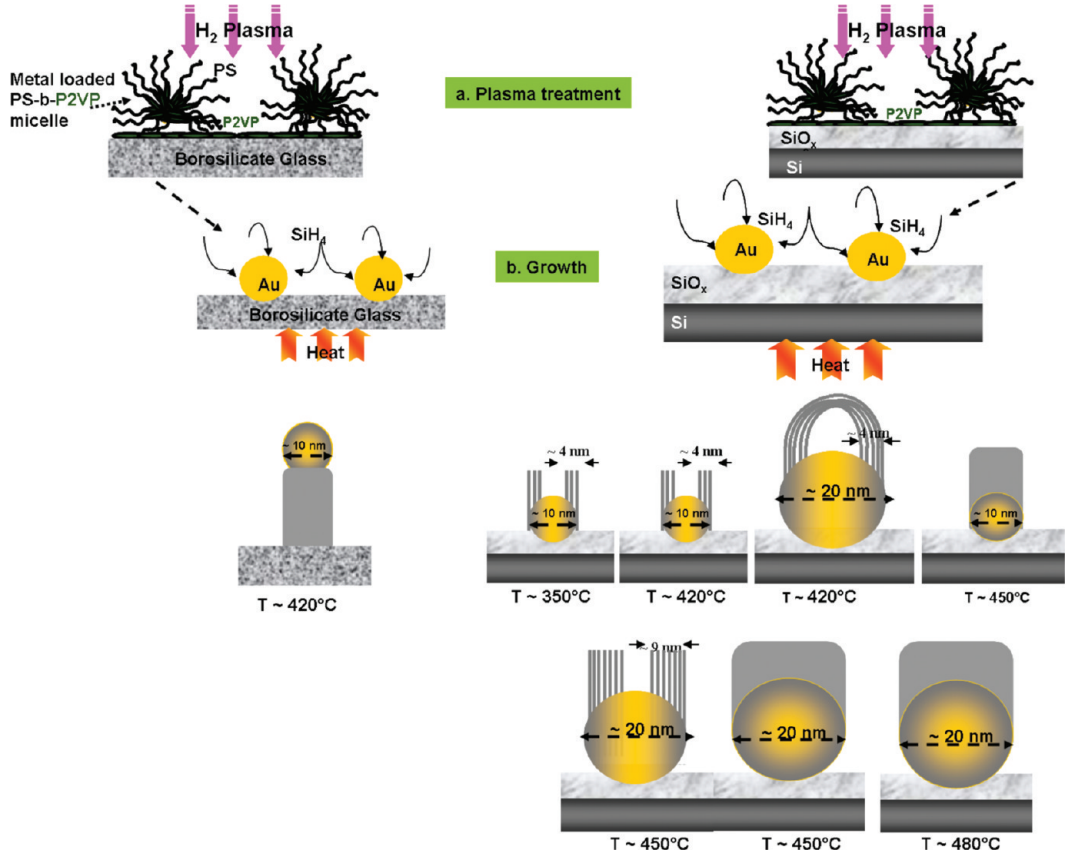

Figure 5. Scheme summarizing the SiNW and SiNT temperature-dependent growth sequences achieved on BSG and SiO_x/Si substrates. Stage a: Au-loaded micelles on both substrates during hydrogen plasma treatment. After removal of the micelle layer, the AuNP is deposited on the BSG substrate but partially embedded in the SiO_x layer of the SiO_x/Si substrate. Stage b: Substrates are heated to the desired growth temperature, and the gaseous precursor starts the growth process. SiNWs that are reasonably aligned at 420 °C are achieved on BSG. On SiO_x/Si, SiNTs with wall thicknesses of ~4−5 nm grow from small NPs up to 420 °C and SiNWs at 450 °C. A mixture of SiNTs (with wall thicknesses of ~9 nm) and SiNWs is acquired at 450 °C from larger NPs and exclusively SiNWs at 480 °C. The scheme at 420 °C is an exemplary illustration of the terminal structure of a SiNT tip after growth completion.

shown in Figure 4f for a 14 nm wide SiNW. Interestingly, from larger NPs ($D > 15$ nm), NTs with wall thicknesses of approximately 9 nm are obtained, as illustrated in Figure 4g,h, for 18 and 22 nm wide SiNTs. Figure 4e,g shows the rounded and closed tips of SiNTs grown at 420 and 450 °C, respectively. The closed and rounded nature of the SiNT tips in this work is analogous to that observed for carbon nanotubes (CNTs) which adopt a root-growth mode.[43,44]

The results show that the micelle nanolithography technique for NP preparation is well-suited for the defined growth of uniform Si 1D features on amorphous substrates. Performing growth below the thermal fragmentation temperature of the silane (~420 °C) enhances the selectivity of the process as side deposition of source material is minimized. While Si 1D growth is only possible at temperatures above 480 °C for NPs prepared in O_2 plasma, the first important observation is that H_2 plasma treatment significantly reduces the process temperature. In comparison to AuNPs of the same diameter (10 nm) treated in O_2 plasma, the Si 1D synthesis temperature is dropped from 550 to 320 °C. This effect has so far been found to be substrate-independent. It is noteworthy that the NPs discussed in this work are in a size range ($d > 10$ nm) above the critical diameter ($d < 6$ nm) below which size-dependent melting of AuNPs becomes eminent, as indicated in the work of Buffat *et al.*[19] As the minimal growth activation temperature of the NPs has so far been independent of the substrate used (also Si and Al_2O_3; not shown here), we believe the catalytic activity observed is pivoted by the plasma atmosphere used during preparation. The data reported here strongly suggests that NP preparation in H_2 plasma significantly enhances their catalytic activity as opposed to NPs of the same size prepared in O_2 plasma. Our observations point toward the fact that AuNP catalytic enhancement comes as a result of impurity atoms incorporated in the NPs from the plasma treatment rather than the NP size. The precise physical phenomena responsible for the enhancement in the catalytic activity for micelle-prepared AuNPs in H_2 plasma remain open and are under investigation.

The growth sequences we observe on both BSG and SiO_x/Si substrates at various temperatures are summarized in the scheme of Figure 5. During plasma treatment, the electric field generated strongly drives mo-

bile carriers in NPs and the energy acquired by them is converted into heat.[45,46] The heat within the NPs as well as its dissipation to the immediate surrounding medium enables the diffusion of the AuNPs into the BSG and or SiO_x matrices (Figure 5a,b). Despite the partial embedding of AuNPs in both BSG and SiO_x matrices, the effective adhesion of the NPs on both substrates is apparently not the same. The existence of nanoscale roughness is known to considerably reduce adhesion between a particle and surface due to a decrease in the real area in contact.[47−49] The differences in surface asperity between the BSG and SiO_x/Si are revealed by our HRTEM studies, as exemplified in Figure 1c,d, whereby the BSG surface reveals more topological roughness (Figure 1c) than the SiO_x/Si (Figure 1d) surface. The tip-growth mode observed on BSG infers a weaker interaction between AuNPs on this substrate than SiO_x/Si on which a root-growth mode prevails within the entire temperature range reported, thus indicating a stronger NP/substrate interaction. Similar observations of difference in growth mode based on surface asperity were made by Song *et al.*,[50] where CNTs grown on different alumina substrates revealed a tip mode for rough surfaces and a root mode for relatively flat surfaces.

From our studies, it is apparent that during growth, even at low temperatures, a tip mode is essential to enable the formation of SiNWs, the reason being that a tip-growth mode enables a uniform diffusion of Si throughout the entire NP. For SiNT formation, however, we perceive that a root mode configuration is necessary. An embedded nanoparticle provides a stronger NP−substrate interaction than an unembedded one. It is conceivable that during growth, the partial embeddment of the NP subjects it to the mechanical constraint of the surrounding substrate, and the diffusion profile of Si within the NP is somewhat affected. This is reflected in the slow growth rate which only led to 200 nm long SiNTs (Figure 2f) as opposed to 2 μm SiNWs obtained on BSG (Figure 2c) at 420 °C.

What we gather so far from the SEM images (Figure 2c,f) is that, in the presented configurations, SiNW growth proceeds at a significantly higher rate than SiNTs. A precise interpretation of the mechanism(s) responsible for SiNT formation is currently not at hand.[51] We however believe that, in our system, the partial embedding of the NP in the SiO_x matrix and failure to dislodge from the substrate during the growth process due to mechanical constraint considerably influence the process, and thereby, on the basis of our current data, we suggest the following model: The significant discrepancies in the thermal expansion coefficients (Au, 14×10^{-6} K^{-1}; and SiO_x, 0.59×10^{-6} K^{-1}) are expected to lead to a build up of biaxial stress on the NP by the substrate. We presume that this stressed state of the NP considerably affects the Si diffusion profile within it. At low temperatures ($T < 420$ °C), the Si diffusion length seems to be limited to about 4 nm, thus enabling the formation of SiNTs from smaller NPs ($D < 15$ nm), as shown in Figure 3a−e. This limitation in Si diffusion length is better perceived in Figure 3e, whereby the inner tube diameter of an 18 nm SiNT (~10 nm) is larger than that of a 14 nm SiNT (~4 nm) obtained at the same growth temperature. The walls of both SiNTs, however, retain an average thickness of ~4 nm. At 450 °C, the Si diffusion length appears to increase to about 9 nm, thus forming SiNWs from small NPs ($D \leq 14$ nm) but SiNTs for larger NPs ($D > 15$ nm) with diameters of 18−22 nm (Figure 3f,g). At 480 °C, only SiNWs occur even for a NP as large as approximately 20 nm (Figure 3f). The Si diffusion lengths provided here are within the range (a few nanometers) of previously reported Si diffusion lengths into a Au film.[52] The rounded nature of the SiNT tips, which resembles those observed in CNTs,[43,44] suggests that they are most likely helical sheets of Si and not hollow cubic crystals of Si as typically observed in template-assisted SiNT growth techniques.[35,39] The coexistence of SiNTs and SiNWs at 450 °C is indicative of a transition temperature where the competitive nature of SiNT and SiNW growth becomes evident. As more NWs than NTs were observed during TEM analysis, we gather that SiNT growth is favored at low temperatures while SiNW formation is dominant at higher temperatures for the NP size range discussed in this work. The growth of the Si 1D structures starts at temperatures well below the Au−Si eutectic point and can be attributed to the decrease of the eutectic temperature for the AuNPs, thus making the vapor−liquid−solid (VLS) mechanism[53] a possible growth process in our system. Alternatively, the vapor−solid−solid (VSS) mechanism[54] may also be responsible for the Si 1D growth at these low temperatures. A concise interpretation is currently not at hand as the influence of H_2 plasma on the physical properties of the NPs is yet to be understood. In addition, the structure and bonding nature of Si in the NTs requires further investigation.

CONCLUSION

In conclusion, we have demonstrated for the first time that, on the basis of AuNPs prepared in H_2 plasma *via* micelle nanolithography, Si 1D growth is enabled on BSG and SiO_x/Si substrates at process temperatures as low as 320 °C. On BSG, for all AuNP sizes discussed here, we acquire SiNWs, which grow in the conventional tip mode as shown in various publications.[54−56] Applying our technique to SiO_x/Si substrates, we have illustrated the controlled synthesis of SiNTs from AuNP seeds, with subsequent high yield, at the lowest temperatures reported so far. SiNT growth is manifested in a temperature window of 320 °C $< T \leq$ 450 °C for AuNPs less than 15 nm in diameter and at $T \approx$ 450 °C for AuNPs within a size range of approximately 16−22 nm. At $T \geq$ 450 °C, SiNW growth is achieved in a root-growth mode for NPs with $D < 15$ nm and at $T \geq$ 480 °C

for NPs up to 22 nm. The micelle technique enables fine control over SiNT size and spacing on SiO_x/Si substrates, which was not achievable *via* previous SiNT growth techniques. Our approach should ease the low-temperature growth and direct integration of Si 1D structures on glassy substrates. The precise control over SiNT diameter will facilitate the exploration of size effects.

METHODS

Nanoparticle Synthesis and Surface Coating. Nanoparticles were prepared *via* micelle nanolithography according to the procedure described in ref 25. Si wafers with a native oxide and BSG surfaces were used as supports for two-dimensional arrays of Au nanoparticles. All surfaces were cleaned in piranha solution, which is a concoction of hydrogen peroxide and sulfuric acid (1:3 H_2O_2/H_2SO_4) for approximately 30 min in order to discard any organic contaminants. The surfaces were subsequently rinsed, sonicated in distilled water, and dried in a stream of nitrogen before the nanoparticle coating process. To coat the surfaces (SiO_x/Si and BSG) with nanoparticles, a monolayer of metal-loaded micelles was brought to all surfaces by dipping a clean, dry surface in a Au-loaded micelle solution at a speed of 12 mm/min. A subsequent treatment in H_2 (0.4 mbar, 250 W) or O_2 (0.1 mbar, 100 W) plasma for 45 min etches away the organic counterpart (micelles), leaving behind the inorganic nanoparticles on the surface in the same quasi-hexagonal order as the initial metal-loaded micelles.

Si 1D Material Growth. Si 1D growth was performed in an Oxford Instruments Plasma Technology Nanofab 700 system. Prior to growth, Au/BSG and Au/SiOx/Si samples were vacuum annealed for 5−20 min at the desired synthesis temperature. After this, monosilane (SiH_4) was flushed into the growth chamber under a constant flow of 40 sccm and a chamber pressure of approximately 2 mbar for 5−15 min depending on the desired length of Si 1D structures. The growth temperature was in the range of 320 to 480 °C. After growth, the samples were then cooled naturally and observed as-grown in a scanning electron microscope. Image quantification was performed with the ImageJ program software.

The temperature values stated here represent those of the heating stage on which a Si carrier wafer (6 in.) was situated. The AuNP-coated sample pieces were subsequently placed on top of the Si carrier wafer prior to all growth experiments. The temperature of the Si carrier wafer is lower than that of the heating stage (displayed temperature) within the gas atmosphere (argon) and pressure (~1 and 5 mbar) conditions of the calibration experiments. At a stage temperature below 400 °C, the difference is in an approximate range of 1−30 °C. With a stage temperature between 400 and 500 °C, the difference is approximately within a 1−50 °C range. The sample pieces are small (max 20 × 20 mm) in comparison to the carrier wafer and thin (300−1000 μm) and were always placed at the center of the carrier wafer. Considering the annealing time provided prior to growth, we assume thermal equilibrium between the Si carrier wafer and the sample pieces during growth.

TEM Specimen Preparation. Cross-sectional TEM samples were prepared using two Si wafers of which one was a dummy and the other the NP structured surface. The samples were glued together on the structured side of the Si wafer and subsequently ground into trapezoidal shapes on each side such that the sample size corresponds to that of a TEM specimen holder. Thin slices of the sandwich structure were cut out using a tungsten wire-saw. The slices were ground from both sides down to a thickness of ~85−95 μm, and subsequently dimpled from one substrate side down to about 30 μm. The minimum thickness depends on the brittle nature of the material being handled. Finally, a small hole is formed in the center of the sample with a low angle ion mill (Gatan PIPS). Specimen regions that are transparent to the electrons are usually found close to the edge of the hole.

Si 1D structures are scrapped into a small container containing an ethanol solution. A dropwise admission of the Si 1D material containing solution onto a TEM grid with a polymer film enables adequate fishing of the Si 1D structures onto the TEM grid. The setback of the technique is the unpleasant aggregation of the Si 1D structures, which renders imaging of an isolated structure difficult. To inhibit Si 1D material aggregation, a TEM grid was pressed on the sample surface and subsequently retracted by peeling off with a pair of tweezers. This way, Si 1D structures stuck onto the grid surface.

Morphology and Structure Characterization. A Zeiss field emission scanning electron microscope (FE-SEM) (Ultra 55), which has an acceleration voltage range up to 30 keV, was used to characterize the morphology of the 1D materials grown. The voltage range used during imaging was typically between 1 and 10 keV.

Structural analysis of the specimen was conducted with a Zeiss 912 Omega energy filtered transmission electron microscope, which was operated at an acceleration voltage of 120 keV. High-resolution TEM (HRTEM) measurements were performed with a JEOL JEM 4000EX, which was operated at an acceleration voltage of 400 keV, as well as the JEOL 1250 ARM, which was operated at an acceleration voltage of 1250 keV.

Acknowledgment. The authors acknowledge the assistance of M. Sycha, T. Dragon, and M. Kelsch in TEM specimen preparation. We appreciate the assistance of P. Kopold and K. Hahn in TEM imaging. We are very grateful to the Max Planck Society for the financial support.

REFERENCES AND NOTES

1. Chen, L. J. Silicon Nanowires: The Key Building Block for Future Electronic Devices. *J. Mater. Chem.* **2007**, *17*, 4639–4643.
2. Nagesha, D. K.; Whitehead, M. A.; Coffer, J. L. Biorelevant Calcification and Non-cytotoxic Behavior in Silicon Nanowires. *Adv. Mater.* **2005**, *17*, 921–924.
3. Hong, K. H.; Kim, J.; Lee, S. H.; Shin, J. K. Strain-Driven Electronic Band Structure Modulation of Si Nanowires. *Nano Lett.* **2008**, *8*, 1335–1340.
4. Hsin, C. L.; Mai, W. J.; Gu, Y. D.; Gao, Y. F.; Huang, C. T.; Liu, Y. Z.; Chen, L. J.; Wang, Z. L. Elastic Properties and Buckling of Silicon Nanowires. *Adv. Mater.* **2008**, *20*, 3919–3923.
5. Il Park, W.; Zheng, G. F.; Jiang, X. C.; Tian, B. Z.; Lieber, C. M. Controlled Synthesis of Millimeter-Long Silicon Nanowires with Uniform Electronic Properties. *Nano Lett.* **2008**, *8*, 3004–3009.
6. Zhang, Z. Y.; Wu, X. L.; Shen, J. C.; Yang, L. W.; Shi, Y.; Chu, P. K.; Siu, G. G. Light Emission from As-Prepared and Oxidized Si Nanowires with Diameters of 5−15 nm. *J. Cryst. Growth* **2005**, *285*, 620–626.
7. Zheng, Y.; Rivas, C.; Lake, R.; Alam, K.; Boykin, T. B.; Klimeck, G. Electronic Properties of Silicon Nanowires. *IEEE Trans. Electron Devices* **2005**, *52*, 1097–1103.
8. Zhang, Z. H.; Liu, H. M.; Xiong, Y. Q.; Xu, W. J.; Tang, Y. H. UV−Vis Absorption and PL Properties of Self-Assembled Silicon Nanotubes. *Chin. Phys. Lett.* **2007**, *24*, 543–545.
9. Lan, J. H.; Cheng, D. J.; Cao, D. P.; Wang, W. C. Silicon Nanotube as a Promising Candidate for Hydrogen Storage: From the First Principle Calculations to Grand Canonical Monte Carlo Simulations. *J. Phys. Chem. C* **2008**, *112*, 5598–5604.
10. Patolsky, F.; Zheng, G. F.; Lieber, C. M. Nanowire-Based Biosensors. *Anal. Chem.* **2006**, *78*, 4260–4269.
11. Wanekaya, A. K.; Chen, W.; Myung, N. V.; Mulchandani, A. Nanowire-Based Electrochemical Biosensors. *Electroanalysis* **2006**, *18*, 533–550.
12. Goncher, G.; Noice, L.; Solanki, R. Bulk Heterojunction Organic−Inorganic Photovoltaic Cells Based on Doped Silicon Nanowires. *J. Exp. Nanosci.* **2008**, *3*, 77–86.

13. Sheu, J. T.; Chen, C. C.; Huang, P. C.; Lee, Y. K.; Hsu, M. L. Selective Deposition of Gold Nanoparticles on SiO_2/Si Nanowires for Molecule Detection. *Jpn. J. Appl. Phys.* **2005**, *44*, 2864–2867.
14. Teo, B. K. Doing Chemistry on Low-Dimensional Silicon Surfaces: Silicon Nanowires as Platforms and Templates. *Coord. Chem. Rev.* **2003**, *246*, 229–246.
15. Xu, S. W.; Lu, Y.; Jiang, Z. Y.; Wu, H. Silica Nanotubes-Doped Alginate Gel for Yeast Alcohol Dehydrogenase Immobilization. *J. Mol. Catal. B* **2006**, *43*, 68–73.
16. Lu, J. Q.; Yi, S. S. Uniformly Sized Gold Nanoparticles Derived from PS-*b*-P2VP Block Copolymer Templates for the Controllable Synthesis of Si Nanowires. *Langmuir* **2006**, *22*, 3951–3954.
17. Buttner, C. C.; Zakharov, N. D.; Pippel, E.; Gosele, U.; Werner, P. Gold-Enhanced Oxidation of MBE-Grown Silicon Nanowires. *Semicond. Sci. Technol.* **2008**, *23*, 075040.
18. Hannon, J. B.; Kodambaka, S.; Ross, F. M.; Tromp, R. M. The Influence of the Surface Migration of Gold on the Growth of Silicon Nanowires. *Nature* **2006**, *440*, 69–71.
19. Buffat, P.; Borel, J. P. Size Effect on Melting Temperature of Gold Particles. *Phys. Rev. A* **1976**, *13*, 2287–2298.
20. Jiang, Q.; Lu, H. M. Size Dependent Interface Energy and Its Applications. *Surf. Sci. Rep.* **2008**, *63*, 427–464.
21. Bahloul-Hourlier, D.; Perrot, P. Thermodynamics of the Au−Si−O System: Application to the Synthesis and Growth of Silicon−Silicon Dioxide Nanowires. *J. Phase Equilib. Diffus.* **2007**, *28*, 150–157.
22. Qi, P. F.; Wong, W. S.; Zhao, H. Z.; Wang, D. W. Low-Temperature Synthesis of Si Nanowires Using Multizone Chemical Vapor Deposition Methods. *Appl. Phys. Lett.* **2008**, *93*, 163101.
23. Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J. F.; Lieber, C. M. Diameter-Controlled Synthesis of Single-Crystal Silicon Nanowires. *Appl. Phys. Lett.* **2001**, *78*, 2214–2216.
24. Fuhrmann, B.; Leipner, H. S.; Hoche, H. R.; Schubert, L.; Werner, P.; Gosele, U. Ordered Arrays of Silicon Nanowires Produced by Nanosphere Lithography and Molecular Beam Epitaxy. *Nano Lett.* **2005**, *5*, 2524–2527.
25. Glass, R.; Arnold, M.; Cavalcanti-Adam, E. A.; Blummel, J.; Haferkemper, C.; Dodd, C.; Spatz, J. P. Block Copolymer Micelle Nanolithography on Non-conductive Substrates. *New J. Phys.* **2004**, *6*, 101.
26. Glass, R.; Moller, M.; Spatz, J. P. Block Copolymer Micelle Nanolithography. *Nanotechnology* **2003**, *14*, 1153–1160.
27. Guczi, L.; Beck, A.; Horvath, A.; Horvath, D. From Molecular Clusters to Metal Nanoparticles. *Top. Catal.* **2002**, *19*, 157–163.
28. Sergeev, G. B. *Nanochemistry*; Elsevier B.V.: Amsterdam, 2006; Chapter 2.
29. Zhang, X. Y.; Whitney, A. V.; Zhao, J.; Hicks, E. M.; Van Duyne, R. P. Advances in Contemporary Nanosphere Lithographic Techniques. *J. Nanosci. Nanotechnol.* **2006**, *6*, 1920–1934.
30. Park, S.; Wang, J. Y.; Kim, B.; Xu, J.; Russell, T. P. A Simple Route to Highly Oriented and Ordered Nanoporous Block Copolymer Templates. *ACS Nano* **2008**, *2*, 766–772.
31. Ross, C. A.; Jung, Y. S.; Chuang, V. P.; Ilievski, F.; Yang, J. K. W.; Bita, I.; Thomas, E. L.; Smith, H. I.; Berggren, K. K.; Vancso, G. J.; Cheng, J. Y. Si-Containing Block Copolymers for Self-Assembled Nanolithography. *J. Vac. Sci. Technol., B* **2008**, *26*, 2489–2494.
32. Colli, A.; Hofmann, S.; Fasoli, A.; Ferrari, A. C.; Ducati, C.; Dunin-Borkowski, R. E.; Robertson, J. Synthesis and Otical Properties of Silicon Nanowires Grown by Different Methods. *Appl. Phys. A* **2006**, *85*, 247–253.
33. Suzuki, H.; Araki, H.; Tosa, M.; Noda, T. Formation of Silicon Nanowires by CVD Using Gold Catalysts at Low Temperatures. *Mater. Today* **2007**, *48*, 2202–2206.
34. Schmidt, O. G.; Eberl, K. Nanotechnology—Thin Solid Films Roll up into Nanotubes. *Nature* **2001**, *410*, 168.
35. Jeong, S. Y.; Kim, J. Y.; Yang, H. D.; Yoon, B. N.; Choi, S. H.; Kang, H. K.; Yang, C. W.; Lee, Y. H. Synthesis of Silicon Nanotubes on Porous Alumina Using Molecular Beam Epitaxy. *Adv. Mater.* **2003**, *15*, 1172–1176.
36. De Crescenzi, M.; Castrucci, P.; Scarselli, M.; Diociaiuti, M.; Chaudhari, P. S.; Balasubramanian, C.; Bhave, T. M.; Bhoraskar, S. V. Experimental Imaging of Silicon Nanotubes. *Appl. Phys. Lett.* **2005**, *86*, 231901.
37. Tang, Y. H.; Pei, L. Z.; Chen, Y. W.; Guo, C. Self-Assembled Silicon Nanotubes under Supercritically Hydrothermal Conditions. *Phys. Rev. Lett.* **2005**, *95*, 116102.
38. Chen, Y. W.; Tang, Y. H.; Pei, L. Z.; Guo, C. Self-Assembled Silicon Nanotubes Grown from Silicon Monoxide. *Adv. Mater.* **2005**, *17*, 564–567.
39. Sha, J.; Niu, J. J.; Ma, X. Y.; Xu, J.; Zhang, X. B.; Yang, Q.; Yang, D. Silicon Nanotubes. *Adv. Mater.* **2002**, *14*, 1219–1221.
40. Xie, M.; Wang, J. S.; Fan, Z. Y.; Lu, J. G.; Yap, Y. K. Growth of P-Type Si Nanotubes by Catalytic Plasma Treatments. *Nanotechnology* **2008**, *19*, 365609.
41. Yamada, S.; Fujiki, H. Experimental Evidence for Nanostructural Tube Formation of Silicon Atoms. *Jpn. J. Appl. Phys.* **2006**, *45*, L837–L839.
42. Kikkawa, J.; Ohno, Y.; Takeda, S. Growth Rate of Silicon Nanowires. *Appl. Phys. Lett.* **2005**, *86*, 123109.
43. Lee, C. J.; Park, J. Growth Model for Bamboolike Structured Carbon Nanotubes Synthesized Using Thermal Chemical Vapor Deposition. *J. Phys. Chem. B* **2001**, *105*, 2365–2368.
44. Kunadian, I.; Andrews, R.; Qian, D. L.; Menguc, M. P. Growth Kinetics of MWCNTs Synthesized by a Continuous-Feed CVD Method. *Carbon* **2009**, *47*, 384–395.
45. Govorov, A. O.; Richardson, H. H. Generating Heat with Metal Nanoparticles. *Nano Today* **2007**, *2*, 30–38.
46. Zeng, N.; Murphy, A. B. Heat Generation by Optically and Thermally Interacting Aggregates of Gold Nanoparticles under Illumination. *Nanotechnology* **2009**, *20*, 375702.
47. Rabinovich, Y. I.; Adler, J. J.; Ata, A.; Singh, R. K.; Moudgil, B. M. Adhesion between Nanoscale Rough Surfaces I. Role of Asperity Geometry. *J. Colloid Interface Sci.* **2000**, *232*, 10–16.
48. Rabinovich, Y. I.; Adler, J. J.; Ata, A.; Singh, R. K.; Moudgil, B. M. Adhesion between Nanoscale Rough Surfaces II. Measurement and Comparison with Theory. *J. Colloid Interface Sci.* **2000**, *232*, 17–24.
49. Tabor, D. Surface Forces and Surface Interactions. *J. Colloid Interface Sci.* **1977**, *58*, 2–13.
50. Song, I. K.; Yu, W. J.; Cho, Y. S.; Choi, G. S.; Kim, D. The Determining Factors for the Growth Mode of Carbon Nanotubes in the Chemical Vapour Deposition Process. *Nanotechnology* **2004**, *15*, S590–S595.
51. Perepichka, D. F.; Rosei, F. Silicon Nanotubes. *Small* **2006**, *2*, 22–25.
52. Lyubinetsky, I. V.; Adamchuk, V. K. Interface Formation During Silicon Deposition on Noble Metal Substrates: A Comparative AES Study. *Thin Solid Films* **1996**, *288*, 182–185.
53. Wagner, R. S.; Ellis, W. C. Vapor-Liquid-Solid Mechanism of Single Crystal Growth (New Method Growth Catalysis from Impurity Whisker Epitaxial + Large Crystals Si E). *Appl. Phys. Lett.* **1964**, *4*, 89.
54. Wang, Y. W.; Schmidt, V.; Senz, S.; Gosele, U. Epitaxial Growth of Silicon Nanowires Using an Aluminium Catalyst. *Nat. Nanotechnol.* **2006**, *1*, 186–189.
55. Lu, W.; Lieber, C. M. Semiconductor Nanowires. *J. Phys. D Appl. Phys* **2006**, *39*, R387–R406.
56. Xie, T.; Schmidt, V.; Pippel, E.; Senz, S.; Gosele, U. Gold-Enhanced Low-Temperature Oxidation of Silicon Nanowires. *Small* **2008**, *4*, 64–68.